Location Optimization of Fault Current Limiter

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Abstract — With the increasing capacity of power systems, fault currents may exceed the interrupting capacity ratings of circuit breakers. Fault current limiters (FCLs) can be applied to maintain circuit breakers within their interrupt ratings. Super conducting fault current limiter (SFCL) have quick response and can operate without auxiliary circuit. For this purpose, rectifier-type superconducting FCL model has been included in short-circuit current analysis and a method to find FCL locations suitable for short-circuit current reduction was proposed. This are validated in IEEE 14 bus system.

Index Terms — Fault Current Limiter, Super Conducting Fault Current Limiter

I. INTRODUCTION

With the increasing demand for power, electric power systems have become greater and are interconnected. As a result, faults in power networks incur large short-circuit currents flowing in the network and in some cases may exceed the ratings of existing circuit breakers (CB) and damage system equipment. To deal with the problem, fault current limiters (FCLs) are often used in the situations where insufficient fault current interrupting capability exists. In this project work a power electronics based fault current limiter will designed and simulated using matlab/simulink model.

Depending on the location of installation, FCL could offer other advantages such as 1) increasing the interconnection of renewable energy and independent power units; 2) increasing the energy transmission capacity over longer distances; 3) reducing the voltage sag caused by the fault; 4) improving the system stability, and 5) improving the system security and reliability.

In radial power systems, the placement of FCL is not difficult, but in loop power system, FCL placement becomes much more complex when more than one location that have high fault current problems. In such a system, short-circuit currents could come from many directions and are not easily blocked by a single FCL. Therefore, from power system operation and planning points of view, a technique that can choose optimum number and locations for FCL placement becoming necessary. For this purpose, rectifier-type superconducting FCL model will included in short-circuit current analysis and a method to find FCL locations suitable for short-circuit current reduction was proposed.

II. SUPER CONDUCTING FAULT CURRENT LIMITER

Before the research and development of the fault current limiter, the main area of research was to break the circuit during fault in order to save the expensive equipment at power grids from large fault currents generated during fault. In order to handle large fault currents circuit breaker with large rating were developed. But the problem with the circuit breakers is that they have a limited life period, and cannot break the circuit until the first current cycle goes to zero. The research amid development of fault current limiters started many years ago. First the basic idea was to limit the fault current so it does not matter if the system is disconnected from supply. Many other methods were used, like air core reactors, basically it was a good approach but the only disadvantage was very high voltage drop in normal operation for which volt-ampere reactive (VAR) compensation was required. The increase in the size of the system is the other disadvantage of this approach. The specifications of the Fault Current Limiter and a description of the limiting behaviour and the installation of the FCL are discussed in [1]. The FCL based on the Microprocessor computer controlled method is discussed in [2]. It consists of an LC circuit tuned to minimum impedance at supply frequency and a thyristor controlled reactor as a shunt which is connected across the capacitor. The current is limited by varying the firing angle of the thyristor due to which the circuit breaker and other protective systems can operate. The sensor and control circuits should operate accurately to detect the fault current. Fault Current Limiter reported in [3] is based on an electromagnetic circuit with iron core and adjustable air gap. Basically the impedance is much less during normal supply operation. During fault the forces produced by the fault current on the plunger causes the inductance of the device to increase. Which limits the current during fault. The proper mechanical movement of the plunger is the main concern. Different approaches of limiting fault current by using PTC thermistors have been explained by Dougal [4]. The results show that the path is good enough to limit the fault current but at the same time the material characteristics need to be known in order for it to work efficiently. The sensor is used to detect the fault current and the action to limit the current is carried out rapidly [5]. This limits the first peak of the fault current.

III. LOCATION OPTIMIZATION OF RESISTIVE TYPE SFCL

In this work resistive type SFCL is used. In order to obtain correct location for SFCL placement, an algorithm is developed and programmed in matlab programming.

Firstly per unit circuit of the power system is modeled. Including sub transient reactance of each synchronous and induction machine.
Z bus is formed using Z bus building algorithm. Power system is assumed to be at no load and voltage at all buses are assumed to be 1 per unit, which will be pre fault voltage $V_f$. We can calculate current at faulted bus $i$ as follows

$$I_{fi} = V_f/Z_i \quad (1)$$

Fault current can be calculated for all buses. Then modification for Zbus can be done in order to place SFCL. SFCL is placed in each line and three phase fault analysis is done. Change in current after the placement of SFCL is calculated. Fig 1 shows the flow chart of location optimization.

**Fig 1 Flow chart for optimal placement of SFCL**

**A. Modification Of Z Bus After Inserting SFCL**

**Fig 2** shows the thevenin equivalent circuit by looking into the system from two existing buses $k$ and $j$. $I_k$ and $I_j$ represents current flowing in to the bus $k$ and $j$. If a FCL with impedance $Z_{FCL}$ were installed on line between bus $k$ and $j$ and fired after the faults, then thevenin equivalent circuit can be represented as shown **Fig 3**

$$Z_p = \frac{Z_j}{Z_{FCL}} \cdot Z_{FCL} \quad (2)$$

Therefore, the modification to the diagonal entries of Zbus after FCL is fired up at a branch between bus $j$ and $k$ is
The fault current deviation at a bus after FCL is fired up can be written as
\[ \Delta I_{i,F} = \frac{V_i}{Z_{ii} + \Delta Z_{ii}} - \frac{V_i}{Z_{ii}} \]  

IV. OPTIMAL PLACEMENT OF SFCL IN IEEE 14 BUS SYSTEM

Based on IEEE 14 bus line data and generator data, Z bus is formed using Z bus building algorithm. Then three phase fault analysis is done in all buses without SFCL to determine fault current. Based on these fault current, buses where fault current to be reduced are identified. SFCL is placed at each line. Modification to Z bus due to SFCL placement is done. Fault current deviation after inserting SFCL is calculated. Optimal location of SFCL can be find out using developed programme. The program is written in matlab. Maximum rating of circuit breaker is assumed as 6 p.u.

Table 2 shows results after fault analysis without SFCL. The results shows that bus 1, 3, 4 have highest fault currents. Which is greater than rating of circuit breaker (ie: 6 p.u). From the results it shows that there is a need for fault current limiter. Further fault analysis is done using matlab programming with inserting SFCL to calculate optimal placement, such that fault current at these buses are reduced.

Table 1 shows fault current deviation in each buses after inserting SFCL. In each line SFCL is inserted then fault current deviation is calculated. Placement of SFCL at line 1 and line 7 has resulted in considerable reduction in fault current whereas Line 7 has highest reduction as shown in the results.

<table>
<thead>
<tr>
<th>Faulted bus</th>
<th>Fault current</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>7.1646</td>
</tr>
<tr>
<td>2</td>
<td>4.2156</td>
</tr>
<tr>
<td>3</td>
<td>6.5908</td>
</tr>
<tr>
<td>4</td>
<td>6.8669</td>
</tr>
<tr>
<td>5</td>
<td>4.8577</td>
</tr>
</tbody>
</table>

From the three phase fault analysis it is identified that fault current at bus 1,3,4 are greater than rating of circuit breaker (ie: 6 p.u). Results shows that by placing SFCL at line 1 or at line 7, fault current at these buses can be reduced within limit (ie: 6 p.u). Whereas line 7 has highest current deviation. Thus line 7 is determined as optimal location.

<table>
<thead>
<tr>
<th>Faulted bus</th>
<th>Fault current</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>2.5205</td>
</tr>
<tr>
<td>7</td>
<td>3.1315</td>
</tr>
<tr>
<td>8</td>
<td>1.9088</td>
</tr>
<tr>
<td>9</td>
<td>2.3858</td>
</tr>
<tr>
<td>10</td>
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<td>11</td>
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<td>12</td>
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<tr>
<td>13</td>
<td>2.3477</td>
</tr>
<tr>
<td>14</td>
<td>1.7277</td>
</tr>
</tbody>
</table>
V. CONCLUSION

The integration of FCLs into power system provides an effective way to suppress large fault currents and may bring to considerable reduction in investment on higher capacity CBs. For a large loop system, its effectiveness would depend on the location of FCL. By using the program developed it is possible to place SFCL at optimal location. Test results have demonstrated the efficiency and accuracy of the proposed method.

REFERENCES