An Area-Efficient High Performance DCT Row/Parallel Architecture for Video Compression

J. Jenet Sheela and G. Sheeba

Abstract--- *A low complexity digital VLSI architecture for the computation of an algebraic integer (AI) based 8-point Arai DCT algorithm is proposed. AI encoding schemes for exact representation of the Arai DCT transform based on a particularly 2-D AI representation is reviewed, leading to the proposed novel architecture based on a new final reconstruction step (FRS) having lower complexity and higher accuracy. The architecture directly realizes an error-free 2-D DCT without using FRSs between row–column transforms, leading to an 8×8 2-D DCT that is entirely free of quantization errors in AI basis. This FRS is based on an optimization derived from expansion factors that leads to small integer constant-coefficient multiplications, which are realized with encoding operation. Efficiencies can be introduced into this method, but the expense of some increase in error. FRS scheme avoiding the leakage of quantization noise between channels. The proposed DCT architecture is able to improve the power consumption and computation speed significantly. This architecture enables low-noise high-dynamic range applications in digital video processing that requires full control of the finite-precision computation of the 2-D DCT. The proposed architectures and FRS techniques are experimentally verified and validated using hardware implementations that are physically realized and verified on field-programmable gate array (FPGA) chip.*

Keywords--- *Algebraic Integer Encoding, DCT, FRS, Compression*

I. INTRODUCTION

THE 8-point discrete cosine transform (DCT) is widely used in video and image compression. However the computational complexity of the DCT operation imparts a heavy burden in VLSI circuits aimed for real time applications.The error free computation of the 8-point DCT using algebraic integer (AI) computation has recently received much attention in the literature as it leads to both low-complexity, low-power consumption and good noise performance. AIs are defined as roots of monic polynomials having integer coefficients. AI based algorithms allow error free computation by eliminating the need of rounding or truncation during the DCT computation.. An AI based exact architecture based on a finite reconstruction step(FRS) algorithm that used the number theoretic method of integer of arithmetic to allow efficient conversion of the AI-encoded DCT coefficient into fixed-point representation. High-Quality digital video in multimedia devices and video-over-Internet protocol (IP) networks connected to the Internet are under exponential growth and, therefore, the demand for applications capable of high dynamic range (HDR) video is accordingly increasing. T Some HDR imaging applications include automatic surveillance [1]–[4], geospatial remote sensing [5], traffic cameras [6], homeland security [4], satellite-based imaging [7], unmanned aerial vehicles [10], automotive industry [13], and multimedia wireless sensor networks. Such HDR video systems operating at high resolutions require an associate hardware capable of significant throughput at allowable area-power complexity.

AI-based procedures for the 2-D DCT are proposed. Their architecture was based on the low-complexity Arai algorithm [3], which formed the building-block of each 1-D DCT using AI number representation. The Arai algorithm is a popular algorithm for video and image-processing applications because of its relatively low computational complexity. Thus, we naturally choose this low complexity algorithm as a foundation for proposing optimized architectures having lower complexity and lower noise. However, such design required the algebraically encoded numbers to be reconstructed to their fixed-point format by the end of column-wise DCT calculation by means of an intermediate reconstruction step. Then data are recoded to enter into the row-wise DCT calculation block [4], This approach is not ideal because it introduces both numerical representation errors and error propagation from the intermediate FRS to the subsequent blocks. We propose a digital hardware architecture for the 8 × 8 2-D DCT capable of: 1) arbitrarily high numeric accuracy, and 2) high throughput. To achieve these goals, our design the signal flow free of quantization errors in all its intermediate computational steps by means of a novel doubly AI encoding concept. No intermediate reconstruction step is introduced and the entire computation truly occurs over the AI structure. This prevents error propagation throughout intermediate computation, which would otherwise result in error correlation among the final DCT coefficients. Thus, errors are totally confined to a single FRS that maps the resulting doubly AI-encoded DCT coefficients into fixed-point representations [14]. This procedure allows the selection of individual levels of precision for each of the 64 DCT spectral components at the FRS. At the same time, such flexibility does not affect noise levels or speed of other sections of the 2-D DCT. The fundamental differences are: 1) the absence of any intermediate reconstruction step; 2) a new doubly AI encoding scheme; and 3) the utilization of a single FRS. The proposed 2-D 8×8

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architecture has the following characteristics: 1) independently selectable precision levels for the 2-D DCT coefficients; 2) total absence of multiplication operations; and 3) absence of leakage of quantization noise between coefficient channels. The proposed architectures aim at performing the FRS operation directly in the bivariate encoded 2-D AI basis.

II. EXISITING SYSTEM

The AI-encoding has been adapted for the VLSI implementation of the 1-D DCT and either trigonometric transforms by Julian et.al in [8]. A unified distributed arithmetic parallel architecture for the computation of DCT and the DST was proposed in [5]. An efficient VLSI linear array for both N-point DCT and inverse discrete cosine transform using a subband decomposition algorithm that results in computational of hardware complexity with FPGA realization is Reported in [7]. A systolic-array algorithm using a memory-based design for both the DCT and the discrete sine transform that is suitable for real-time VLSI realization was proposed in [13]. An FPGA based system-on-chip realization of the 2-D DCT for 8x8 block size that operates at 107MHZ with a latency of 80 cycles is available in [9]. AI- based realization on the row-wise & column-wise application of 1-D DCT cores that employ AI quantization in [6]. A Low-complexity core for quantized 8x8/4x4 combined with MPEG4 codecs and FPGA synthesis is available in [4]. An efficient VLSI Linear array for DCT processor with the computation complexity and hardware complexity is fully pipelined and scalable for variable length DCT/IDCT computation in [2]. Minimum number of additions is used to compute the 2-D DCT by Yanling chen et al in [1]. Although employs AI encoding, it is not an error-free architecture.

III. PROPOSED SYSTEM

An 8 × 8 image block has its 2-D DCT transform mathematically expressed by [1]

$$(C{\cdot}(C{\cdot}A)^{T\ T}) \qquad (1)$$

where C is the usual DCT matrix [2]. It is straightforward to notice that this operation corresponds to the column-wise application of the 1-D DCT to the input image **A**, followed by a transposition, and then the row-wise application of the 1-D DCT to the resulted matrix.

The proposed architecture consists of five subcircuits [7]:

1. an input decimator circuit;
2. an eight-point AI-encoded 1-D DCT block shown in
3. Fig. 1, which performs column-wise computation based
4. on the Arai algorithm [13] and furnishes the intermediate
5. result **C** · **A** in the AI domain;
6. an AI-based transposition buffer shown in Fig. 2 with a
7. wired cross-connection block for obtaining (**C** · **A**)*T* ;
8. four parallel instantiations of the same eight-point AI based Arai DCT block in Fig. 1 for row-wise computation
9. of eight 1-D DCTs, which results in **C** · (**C** · **A**)*T* ;
10. an FRS circuit for mapping the AI-encoded 2-D DCT coefficients to 2's complement format.

A. Bit Serial Data Input, Ser-Des, and Decimation

We assume that the input video data, in raster-scanned format, has already been split into 8×8 pixel blocks. We further assume that these blocks can be stacked to form an eight-column and (8 × (number of blocks))-row data structure. This leads to so-called "blocked" video frames, each of size 8 × 8 pixels. The blocking procedure leads to a raster scanned sequence of pixel intensity (or color) values x_{in} ,i = 0, 1, . . . , 7, n = 0, 1, . . . , 8 × (number of blocks) − 1, from an 8 × 8-blocked image. Note that we use column–row order for the indexes, instead of row–column. Due to the 8 × 8 size of the 2-D DCT computation, we find it quite convenient to consider the time index n after a modular operation $k \equiv n$ (mod 8). Hereafter, we will refer to the time index as a modular quantity k = 0, 1, . . . , 7, 0, 1, . . . , 7, 0, 1, . . . , 7, ... The video signal is serially streamed through the input port of the architecture at a rate of Fs . A bit serial port connected to a serializer/deserializer (Ser/Des) is required to be fed using a bit rate of 8 × Fs without considering overheads.

Following the Ser/Des, a decimation block converts the input byte sequence into a row structure by means of delaying and down sampling by eight as shown in Fig.1.he last transposition (3) is obtained via wired cross connections. The proposed architecture is shown in Fig. 1.

B. Eight-Point AI-Encoded Arai DCT Core

The column-wise transform operation is performed according to the eight-point AI-based Arai DCT hardware cores as designed in [1] and [2] shown in Fig. 1. Here, this scheme is employed with the *removal* of its original FRS.

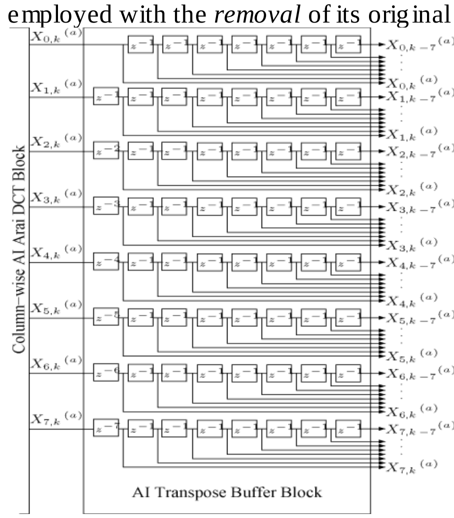

Fig. 1: 1-D AI transpose buffer used in Fig. 3

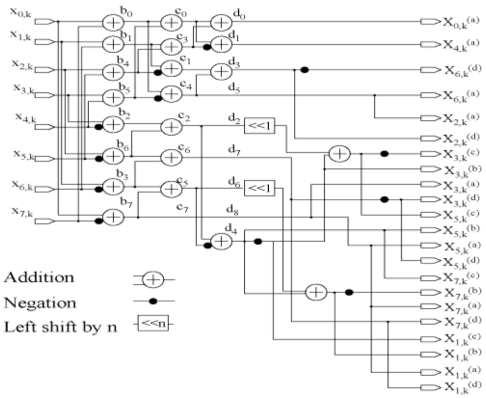

Fig.2. 1-D AI Arai DCT block used in Fig. 3.

In practical terms, a good AI representation possesses a basis such that: 1) the required constants can be represented *without* error; 2) the integer elements provided by the representation are sufficiently small to allow a simple architecture design and fast signal processing; and 3) the basis itself contains few elements to facilitate simple encoding–decoding operation.

C. Real-Time AI-TB

The proposed AI-TB consists of a chain of clocked first- in-first-out (FIFO) buffers for each AI-based channel of each component of the column-wise transformation [11]. For each parallel integer channel q, there are eight FIFO taps clocked at rate F_{clock} . Therefore, the set of FIFO buffers leads to 22 × 8 = 176 output ports from the FIFO buffer section. Hard wired cross-connections are used that physically realize the required transpose matrix for the next row-wise DCT section.

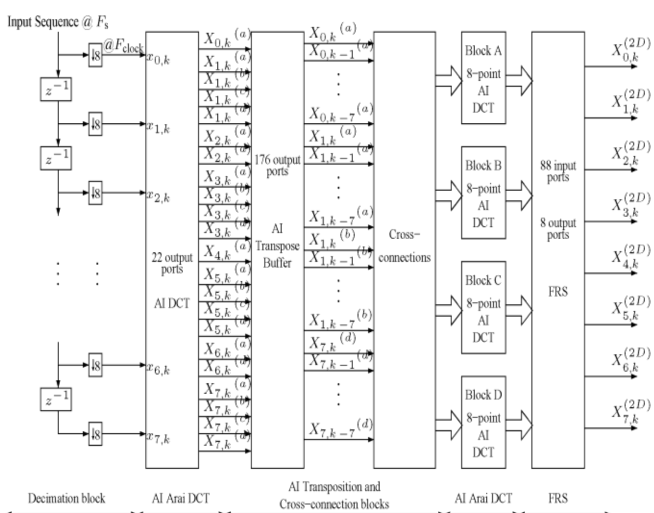

Fig. 3. Proposed 2-D AI-DCT architecture

D. Row-Wise DCT Computation

The cores are set in parallel being able to compute an eight-point DCT every eight clock cycles of the master clock signal. This operation performs the required row-wise DCT computation.

E. Final Reconstruction Step

The final stage of the 1-D AI encoding based DCT architecture is the FRS which is used for converting the computed DCT coefficients from the infinite precision AI encoding into fixed-point representation. From [1], such conversions require the multiplication of each AI encoded output value with the finite precision approximation corresponding to each AI basis. Consider the set of 2-D AIs used in [1]. As shown in Figure 3, FRS using 2-D AI encoding technique, not only have we achieved significant improvement in quality of reconstructed image but the hardware is also greatly reduced. In this paper, we propose a scheme for realization of a low complexity high-accuracy FRS using number theoretical approximations based on *AI Encoding* [9]. This would facilitate the usage of integer arithmetic in place of fixed-point. Such approach has been often employed by integer transform designers [4]. Furthermore, the final precision for the DCT block depends solely on the FRS, which is quite flexible.

IV. RESULTS AND DISCUSSIONS

Experiments are conducted on High-Quality digital video in multimedia devices. AI encoding is used on the Arai fast algorithm for DCT computation, and a novel FRS structure based on AI encoding is employed. By the use of AI encoding the optimum circuits are synthesized for FRS structures corresponding to two suitable arithmetic integers. FRS uses an observation of zero terms in the algebraic integer (AI) representation of the odd and even angle functions.

For the computation in algebraic integer representation, only 8 to 16 bit adders are needed. Furthermore, the final precision for the DCT block depends on the FRS, which is quite flexible. It features the fastest operating speed and the smallest area with its sufficiency accuracy satisfying the practical application.

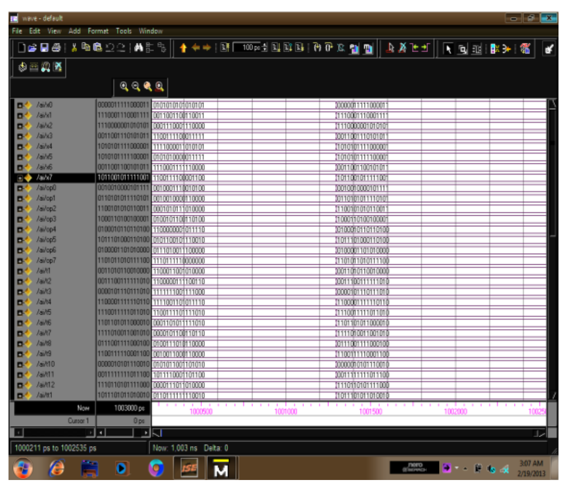

Figure 4. Results for AI-encoding

V. Conclusion and Future Work

Today's design engineers are focusing a growing need to conserve power. To meet low power requirements, they require a comprehensive, robust low power design services to help them meet their toughest design challenges. This paper is based on number of research articles published in the last two decades and periodic updates on error free 2-D DCT architecture, which will be useful as new practices continue to evolve in the field of video compression. A time-multiplexed row parallel hardware architecture was proposed for the real-time computation of the bivariate AI- encoded 2-D Arai DCT. The architecture was the first 2-D AI-encoded DCT hardware that operated completely in the AI domain. This makes the proposed system not only completely multiplier-free but also quantization free up to the final output channels.

In future add/sharing technique can be implemented to FRS block. This technique avoid the interfere between two channels. This technique enables low-noise high-dynamic range applications in digital video processing that requires full control of the finite-precision computation of the 2-D DCT**.**

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